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User Manual

PMC-PARALLEL-485
Version Standard

Digital Parallel Interface
PMC Module

Revision C
Corresponding Hardware: Revision 2
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PMC-PARALLEL-485

Digital Parallel Interface
PMC Module

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This product has been designed to operate with PMC Module carriers and compatible user-provided equipment. Connection of incompatible hardware is likely to cause serious damage.

Manual Revision A. Revised 4/30/03

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Product Description

PMC-PARALLEL-485 is part of the PCI Mezzanine Card [PMC] family of modular I/O components. The PMC-PARALLEL-485 provides 32 differential IO lines in one PMC slot. The IO lines are brought to a 68-pin SCSI 3 style connector and to the backplane connector. In addition, a bi-directional clock and clock enable differential pair are provided at the front panel.

Each of the 32 differential pairs is programmable to be an input or an output. The lower 4 bits [0-3] are individually programmable. The remaining bits are programmed on a nibble basis. Input, Output, Termination active or disabled.

The IO are available as inputs in two forms. The data can be read directly without filtering or from a data latch which captures any detected 'hi' condition. The data can be selectively inverted and masked prior to the latch function. The data latches can be programmed to respond to a rising or falling edge, or simply to the voltage level of the signal. The direct read data is unaffected by the inversion, filtering, and masking. The output lines are driven, double clocked, from the output register.

The 485 transceivers are selectively enabled for transmitting and always enabled for receiving. Separate input and output lines between the FPGA and the transceivers allow for local loop-back if the transceivers are enabled to transmit.

Each differential pair has a 180Ω parallel termination resistor. Analog switches are programmed to activate the termination when the termination bit for an IO pair is set. The resistance stated includes the analog switch contribution. For cable terminated environments the analog switches and resistors can be programmed to be disabled.

Eight “user bits” are supplied for user configuration control.

A clock generator is provided which can be referenced to an external source, the local oscillator [optional] or the PCI clock. The generator has a programmable divider [12 bits].

All configuration registers support read and write operations for maximum software convenience. LW operations are supported (please refer to the memory map).

The PMC-PARALLEL-485 conforms to the PMC standard. This guarantees compatibility with multiple PMC Carrier boards. Because the PMC may be

mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one PMC Carrier board, with final system implementation on a different one.

Theory of Operation

The PMC-PARALLEL-485 is a part of the PMC family of modular I/O products. It meets the PMC Module Standard. It is assumed that the reader is at least casually familiar with this document and logic design.

The PMC-PARALLEL-485 is designed for the purpose of transferring data from one point to another with a parallel protocol. The PMC-PARALLEL-485 features a Xilinx FPGA and 34 differential transceivers. The transceivers can be programmed to be drivers or receivers. The terminations can be programmed to be active or disabled. The controls are individual for IO 0-3 and by groups of four IO for IO 4-31. The clock and clock enable have a common direction control. The FPGA contains the PCI interface and control required for the parallel interface.

The PCI interface is achieved with the Xilinx Core design. The Xilinx design requires 1 wait state for read or write cycles to any address. Data remains enabled during a read until the data is read in by the PCI core interface.

Three registers are used to interact with the basic data interface. The output data register [pmc_par485_dataout] is connected to the driver side of the '485 transceiver. The input register [pmc_par485_datain] is read-able from the host and is connected to the receive side of the transceiver. The direction register [pmc_par485_dir_term] has a bit corresponding to each IO or nibble group which controls the direction of each transceiver. The direction controls default to read. The terminations are programmed through the same register.

If set to drive the bus then the value driven corresponds to the bit in the output data register. The output data register is read-writeable and because the register is independent of the bus, the data read will always match the data written allowing read-modify-write operations. The separate input register provides access to the IO bus side of the drivers. The data read will reflect the state of the bus and not necessarily the state of the on-board drivers. Please see the connector definitions and register descriptions for more details.

The input data is registered and clocked with the PCI bus clock. The data is available "as-is" via the "datain" register. A filtered version of the data is available from the "datain_lat" register. Each data input line has three corresponding filter control bits one in each of the "pol", "edge/level", and "mask" registers. The "pol" register controls inversion of the input data. The "edge/level" register controls whether the latch responds to a rising or

falling edge (controlled by the "pol" setting) or the voltage level of the signal. The "mask" register controls which bits can be latched by the data latch. Once a filtered data bit is captured the data is held in the latch until cleared. The latch is cleared on a bit selectable basis by a write to the latch. The bits that are written as ones will be cleared until new data is detected.

The onboard clock generator can utilize an external clock, the PCI clock or the onboard reference oscillator [optional] as a clock source. Further the generator can be programmed to divide the reference down to provide a useful frequency. The "base" control register controls the operation of the generator, the clock enable and external clock direction.

The interrupt sources correspond to the data bits that are selected to be latched. The interrupt state is available masked and unmasked in the "stat" register to allow polling and interrupt priority processing. In addition an extra signal [force int] is supplied to allow software generated interrupts for development and debugging purposes. The master interrupt enable and force interrupt bits are also located in the "base" control register.

Programming

Programming the PMC-PARALLEL-485 requires only the ability to read and write data in the host's PMC space. The base address is determined by the PMC Carrier board. This documentation refers to the address of the PMC space, for the slot that the PMC is installed in, as the base address.

Refer to the Theory of Operation section above and the Interrupts section below for more information regarding the exact sequencing and interrupt definitions.

The PMC_Parallel_485 has a VendorID of 0x10EE and a CardID of 0x0009. The current revision is 0x00. Your driver can use the configuration information to identify the PMC_Parallel_485 during initialization in systems where address spaces are allocated dynamically.

Address Map

```
  Function                Offset   Function
// PMC  relative addresses //
#define pmc_par485_base        0x00  // clock and interrupt control
#define pmc_par485_stat        0x04  // interrupt status
#define pmc_par485_eg_lvl      0x08  // data latch edge or level control
#define pmc_par485_mask        0x0C  // data latch mask register
#define pmc_par485_pol         0x10  // data in polarity selection reg.
#define pmc_par485_dir_term    0x14  // direction and termination reg.
#define pmc_par485_dataout     0x18  // output data register
#define pmc_par485_datain      0x24  // data input register
#define pmc_par485_datain_lat  0x28  // data input latched register
#define pmc_par485_sw          0x44  // read the user dip switch setting
```

FIGURE 1 PMC-PARALLEL-485 INTERNAL ADDRESS MAP

The address map provided is for the local decoding performed within PMC-PARALLEL-485. The addresses are all offsets from a base address. The carrier board, that the PMC is installed into, provides the base address.

Register Definitions

pmc_par485_base

[$00] parallel-485 Base Control Port read / write

BASE CONTROL REGISTER

DATA BIT	DESCRIPTION
31-20	Spare
19	Master Interrupt Enable
18	Force Interrupt
17	Enable Select
16	Clock Enable
15	External Clock Direction
14-13	Clock Pre-Selector
12	Clock Post-Selector
11-0	Divisor

FIGURE 2 PMC-PARALLEL-485 BASE CONTROL BIT MAP

The PS [pre-selector] bits are used to select from the clock sources.
00 = '0' no clock
01 = Oscillator – (Optional - Frequency selectable)
10 = External Clock - received from an RS 485 differential pair
11 = PCI Clock

Divisor [11-0] are the clock divisor select bits. The clock source is divided by a counter and the select bits pick which clock is used to drive the divider network and the clock output. The reference clock for the counter is selected with the CLK Pre-Selector. The output frequency is {reference / [2(n+1)]}. N≥1. The reference oscillator frequency is user selectable. The counter divides by N+1 due to counting from 0 ->n before rolling over. The output is then divided by two to produce a square wave output.

Post Selector when '1' sets clock out to the divided clock, when '0' sets clock out to pre-selector referenced clock.

Please note that the 485 buffers are rated for a guaranteed maximum of 12 MHz.

The external clock direction bit controls the direction of the external clock and clock enable drivers. When this bit is a '1' these drivers are configured as outputs, otherwise they are inputs.

The clock enable bit is the internal source for enabling the output clock. When this bit is a '1' the clock is enabled except when the external clock enable is being used.

The enable select bit selects the enable source when the external clock drivers are configured as inputs. When this bit is a '1' the external enable input is used to enable the clock, otherwise the clock enable bit performs this function (see above).

The force interrupt bit is used to generate an interrupt condition regardless of input data levels.

The master interrupt enable bit enables the interrupt onto the PCI bus. When this bit is a '1' and an interrupt condition exists, a system interrupt is generated.

pmc_par485_stat

[$04] parallel-485 Status Port read only

STATUS REGISTER

DATA BIT	DESCRIPTION
31-2	Spare
1	Interrupt Out
0	Interrupt Status

FIGURE 3 PMC-PARALLEL-485 STATUS BIT MAP

The Status register provides a read-only port for interrupt status.

The interrupt status bit, when '1', indicates that an interrupt condition exists, either from input data conditions, or the force interrupt bit.

The interrupt out bit, when '1', indicates that a system interrupt is asserted. This occurs when both an interrupt condition exists and the master enable bit is asserted.

pmc_par485_eg_lvl

[$08] parallel-485 Edge / Level Control Register Port read / write

CONTROL REGISTER EDGE / LEVEL	
DATA BIT	**DESCRIPTION**
31-0	Edge Enable

FIGURE 4 PMC-PARALLEL-485 EDGE/LEVEL CONTROL BIT MAP

When an edge enable bit is a '1', the corresponding data bit will be latched when an edge occurs, provided its mask bit is enabled. If the bit is a '0', the level of the signal is used. The polarity of the edge or level depends on the state of the corresponding bit in the polarity register.

pmc_par485_mask

[$0C] parallel-485 Mask Port read / write

CONTROL REGISTER MASK	
DATA BIT	**DESCRIPTION**
31-0	1 = enable, 0 = mask off for data input latch

FIGURE 5 PMC-PARALLEL-485 MASK CONTROL BIT MAP

If an input bit is desired to be monitored then the corresponding mask bit should be set to '1'. To keep an input bit from being active, set the corresponding bit to '0'.

pmc_par485_**pol**

[$10] parallel-485 Polarity Port read / write

CONTROL REGISTER POLARITY	
DATA BIT	**DESCRIPTION**
31-0	1 = invert, 0 = normal

FIGURE 6 PMC-PARALLEL-485 POLARITY CONTROL BIT MAP

If an input bit is active low then the corresponding polarity bit should be set to '1'. The data input latch will capture the level of a signal. Active low signals should be inverted to capture the active state. If the corresponding

edge enable bit is set, then a '1' indicates a falling edge and a '0' indicates a rising edge.

pmc_par485_dir_**term**

[$14] parallel-485 direction and termination Port read / write

CONTROL REGISTER DIR_TERM

DATA BIT	DESCRIPTION
10-0	DIRection 10-0 0 = tristate, 1 = drive
26-16	TERMination 10-0 1 = terminated

FIGURE 7 PMC-PARALLEL-485 DIRECTION TERMINATION CONTROL BIT MAP

The direction for each of the 32 differential pairs is controlled through this port. The port defaults to '0' which corresponds to tri-stating the drivers. The output and input pins are separated and independently connected to the Xilinx to allow loop-back testing. The input side is always active.

Pull-up and Pull-down resistors built into some '485 interface devices may make the signal appear to be driven [if open] when in the tri-stated mode. Enabling the termination on a tristated line will yield approximately 2.5V on each side of the tri-stated driver.

CONTROL	CORRESPONDING IO BIT(S)
DIR_0..3	IO_0..3.
DIR4	IO_4..7
DIR5	IO_8..11
DIR6	IO_12..15
DIR7	IO_16..19
DIR8	IO_20..23
DIR9	IO_24..27
DIR10	IO_28..31

Parallel termination resistors are supplied on each differential pair along with a switch to allow the user to select which lines are terminated and where. In some systems it will make sense to terminate the lines in the cable and in others it will make sense to use the onboard terminations.

CONTROL	CORRESPONDING IO BIT(S)
TERM_0..3	IO_0..3.
TERM4	IO_4..7
TERM5	IO_8..11
TERM6	IO_12..15
TERM7	IO_16..19
TERM8	IO_20..23
TERM9	IO_24..27
TERM10	IO_28..31

pmc_par485_**dataout**

[$18] parallel-485 Write Port read / write

CONTROL REGISTER DATA OUT	
DATA BIT	**DESCRIPTION**
31-0	IO31-IO0

FIGURE 8 PMC-PARALLEL-485 DATAOUT BIT MAP

The 32 bits are written through this port. The port is on the single ended side of the transceivers. The data read will match the data written to this port because the Xilinx internal register is being read.

The data written to this port is double-clocked with the inverted output clock, therefore this data will appear on the output drivers within two clock periods of being written, provided the clock is enabled.

pmc_par485_datain

[$24] parallel-485 data input read only

DATA INPUT PORT	
DATA BIT	**DESCRIPTION**
31-0	Value currently on data input lines

FIGURE 9 PMC-PARALLEL-485 DATA IN BIT MAP

The "natural" data from the input port is available on this port. The data input lines are continuously sampled with Xilinx input flip-flops at the PCI clock rate. When a read occurs the value on the flip-flops is returned to the host.

pmc_par485_**datain_lat**

[$28] parallel-485 data input latch / clear latch read / write

LATCHED DATA INPUT PORT	
DATA BIT	**DESCRIPTION**
31-0	Value in input data latch

FIGURE 10 PMC-PARALLEL-485 DATA IN LATCHED BIT MAP

The filtered and captured input data is available from this port. This data can be read as many times as desired; the data is cleared by writing a '1' to the bit that is to be cleared . See the Polarity, Edge / Level and Mask registers for more details on the filtering capabilities.

pmc_par485_sw

[$44] Parallel-485 Switch Read Port read only

USER SWITCH PORT	
DATA BIT	**DESCRIPTION**
7	UB7
6	UB6
5	UB5
4	UB4
3	UB3
2	UB2
1	UB1
0	UB0

FIGURE 11 PMC-PARALLEL-485 SWITCH READ BIT MAP

The Switch Read Port has the user bits. The user bits are connected to 8 switch positions. The switches allow custom configurations to be defined by the user and for the software to “know” how to configure the read / write capabilities of each IO line.

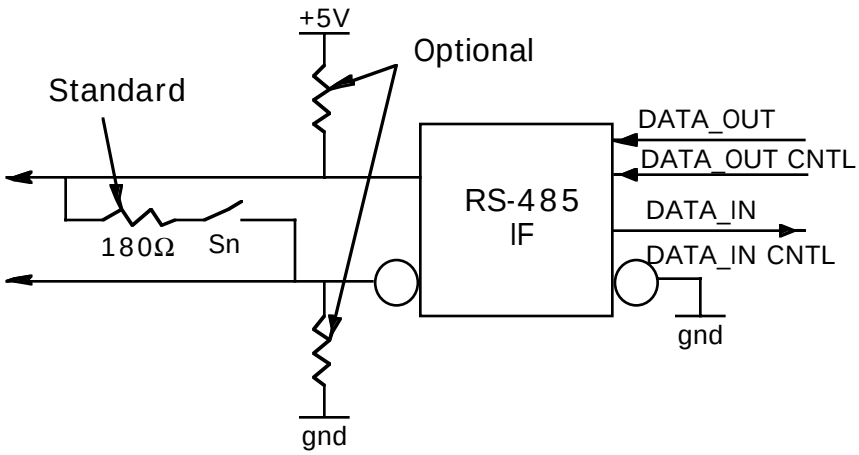

FIGURE 12 PMC-PARALLEL-485 TERMINATION

The PMC-PARALLEL-485 design layout provides for a variety of termination options. The standard termination is for programmable 180Ω parallel. Factory options include:
1) different parallel termination values
2) pull-up / pull-down resistors
3) Fused 3.3V reference
4) ground references
5) special circuit which receives one differential pair which is then driven out on two differential pairs and one open drain circuit.

The first two options are available on all IO pairs. The 3rd, 4th, and 5th options are restricted to certain pins. Please refer to the "Alternate" pin definitions in the next section of this document. Please contact Dynamic Engineering if an alternate configuration is needed for your project.

PMC Module Logic Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn1 Interface on the PMC-PARALLEL-485. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification and not needed by this design.

	-12V	1	2
GND	INTA#	3	4
		5	6
BUSMODE1#	+5V	7	8
		9	10
GND -		11	12
CLK	GND	13	14
GND -		15	16
	+5V	17	18
	AD31	19	20
AD28-	AD27	21	22
AD25-	GND	23	24
GND -	C/BE3#	25	26
AD22-	AD21	27	28
AD19	+5V	29	30
	AD17	31	32
FRAME#-	GND	33	34
GND	IRDY#	35	36
DEVSEL#	+5V	37	38
GND	LOCK#	39	40
		41	42
PAR	GND	43	44
	AD15	45	46
AD12-	AD11	47	48
AD9-	+5V	49	50
GND -	C/BE0#	51	52
AD6-	AD5	53	54
AD4	GND	55	56
	AD3	57	58
AD2-	AD1	59	60
	+5V	61	62
GND		63	64

FIGURE 13 PMC-PARALLEL-485 PN1 INTERFACE

PMC Module Logic Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn2 Interface on the PMC-PARALLEL-485. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification and not needed by this design.

+12V		1	2
		3	4
	GND	5	6
GND		7	8
		9	10
		11	12
RST#	BUSMODE3#	13	14
	BUSMODE4#	15	16
	GND	17	18
AD30	AD29	19	20
GND	AD26	21	22
AD24		23	24
IDSEL	AD23	25	26
	AD20	27	28
AD18		29	30
AD16	C/BE2#	31	32
GND		33	34
TRDY#		35	36
GND	STOP#	37	38
PERR#	GND	39	40
	SERR#	41	42
C/BE1#	GND	43	44
AD14	AD13	45	46
GND	AD10	47	48
AD8		49	50
AD7		51	52
		53	54
	GND	55	56
		57	58
GND		59	60
		61	62
GND		63	64

FIGURE 14 PMC-PARALLEL-485 PN2 INTERFACE

PMC Module Front Panel IO Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module IO Interface on the PMC-Parallel_485. Also see the User Manual for your carrier board for more information.

EXT_CLK_ENP	EXT_CLK_ENN	1	35
EXT_CLKP	EXT_CLKN	2	36
IO_0P	IO_0N	3	37
IO_1P	IO_1N	4	38
IO_2P	IO_2N	5	39
IO_3P	IO_3N	6	40
IO_4P	IO_4N	7	41
IO_5P	IO_5N	8	42
IO_6P	IO_6N	9	43
IO_7P	IO_7N	10	44
IO_8P	IO_8N	11	45
IO_9P	IO_9N	12	46
IO_10P	IO_10N	13	47
IO_11P	IO_11N	14	48
IO_12P	IO_12N	15	49
IO_13P	IO_13N	16	50
IO_14P	IO_14N	17	51
IO_15P	IO_15N	18	52
IO_16P	IO_16N	19	53
IO_17P	IO_17N	20	54
IO_18P	IO_18N	21	55
IO_19P	IO_19N	22	56
IO_20P	IO_20N	23	57
IO_21P	IO_21N	24	58
IO_22P	IO_22N	25	59
IO_23P	IO_23N	26	60
IO_24P	IO_24N	27	61
IO_25P	IO_25N	28	62
IO_26P	IO_26N	29	63
IO_27P	IO_27N	30	64
IO_28P	IO_28N	31	65
IO_29P	IO_19N	32	66
IO_30P	IO_30N	33	67
IO_31P	IO_31N	34	68

FIGURE 15 PMC-PARALLEL-485 FRONT PANEL INTERFACE STANDARD

PMC Module Backplane IO Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module IO Interface on the PMC-Parallel_485 and routed to Pn4. Also see the User Manual for your carrier board for more information.

IO_0P	IO_0N	1	2
IO_1P	IO_1N	3	4
IO_2P	IO_2N	5	6
IO_3P	IO_3N	7	8
IO_4P	IO_4N	9	10
IO_5P-	IO_5N	11	12
IO_6P-	IO_6N	13	14
IO_7P-	IO_7N	15	16
IO_8P-	IO_8N	17	18
IO_9P-	IO_9N	19	20
IO_10P-	IO_10N	21	22
IO_11P-	IO_11N	23	24
IO_12P-	IO_12N	25	26
IO_13P-	IO_13N	27	28
IO_14P-	IO_14N	29	30
IO_15P-	IO_15N	31	32
IO_16P	IO_16N	33	34
IO_17P	IO_17N	35	36
IO_18P	IO_18N	37	38
IO_19P	IO_19N	39	40
IO_20P-	IO_20N	41	42
IO_21P-	IO_21N	43	44
IO_22P-	IO_22N	45	46
IO_23P-	IO_23N	47	48
IO_24P-	IO_24N	49	50
IO_25P	IO_25N	51	52
IO_26P	IO_26N	53	54
IO_27P	IO_27N	55	56
IO_28P	IO_28N	57	58
IO_29P-	IO_29N	59	60
IO_30P-	IO_30N	61	62
IO_31P-	IO_31N	63	64

FIGURE 16 PMC-PARALLEL-485 PN4 INTERFACE STANDARD

PMC Module Front Panel IO Alternate Pin Assignment

The figure below gives the pin assignments for the PMC Module IO Interface on the PMC-Parallel_485. These are the alternate pin definitions. Also see the User Manual for your carrier board for more information.

EXT_CLK_ENP	EXT_CLK_ENN	1	35
EXT_CLKP	EXT_CLKN	2	36
3.3V	3.3V	3	37
gnd	gnd	4	38
gnd	gnd	5	39
RSTINP	RSTINN	6	40
RSTOUT1P	RSTOUT1N	7	41
RSTOUT2P	RSTOUT2N	8	42
RESET*	UNUSED	9	43
IO_7P	IO_7N	10	44
CLK1P	CLK1N	11	45
RST1P	RST1N	12	46
CLK2P	CLK2N	13	47
RST2P	RST2N	14	48
IO_12P	IO_12N	15	49
IO_13P	IO_13N	16	50
IO_14P	IO_14N	17	51
IO_15P	IO_15N	18	52
IO_16P	IO_16N	19	53
IO_17P	IO_17N	20	54
IO_18P	IO_18N	21	55
IO_19P	IO_19N	22	56
IO_20P	IO_20N	23	57
IO_21P	IO_21N	24	58
IO_22P	IO_22N	25	59
IO_23P	IO_23N	26	60
IO_24P	IO_24N	27	61
IO_25P	IO_25N	28	62
IO_26P	IO_26N	29	63
IO_27P	IO_27N	30	64
IO_28P	IO_28N	31	65
IO_29P	IO_29N	32	66
IO_30P	IO_30N	33	67
IO_31P	IO_31N	34	68

FIGURE 17 PMC-PARALLEL-485 FRONT PANEL INTERFACE ALTERNATE

PMC Module Backplane IO Alternate Pin Assignment

The figure below gives the pin assignments for the PMC Module IO Interface on the PMC-Parallel_485 and routed to Pn4. These are the alternate pin assignments. Also see the User Manual for your carrier board for more information.

3.3V	3.3V	1	2
GND	GND	3	4
GND	GND	5	6
RSTINP	RSTINN	7	8
RSTOUT1P	RSTOUT1N	9	10
RSTOUT2P	RSTOUT2N	11	12
RESET*	UNUSED	13	14
IO_7P	IO_7N	15	16
CLK1P	CLK1N	17	18
RST1P	RST1N	19	20
CLK2P	CLK2N	21	22
RST2P	RST2N	23	24
IO_12P	IO_12N	25	26
IO_13P	IO_13N	27	28
IO_14P	IO_14N	29	30
IO_15P	IO_15N	31	32
IO_16P	IO_16N	33	34
IO_17P	IO_17N	35	36
IO_18P	IO_18N	37	38
IO_19P	IO_19N	39	40
IO_20P	IO_20N	41	42
IO_21P	IO_21N	43	44
IO_22P	IO_22N	45	46
IO_23P	IO_23N	47	48
IO_24P	IO_24N	49	50
IO_25P	IO_25N	51	52
IO_26P	IO_26N	53	54
IO_27P	IO_27N	55	56
IO_28P	IO_28N	57	58
IO_29P	IO_29N	59	60
IO_30P	IO_30N	61	62
IO_31P	IO_31N	63	64

FIGURE 18 PMC-PARALLEL-485 PN4 INTERFACE ALTERNATE

Applications Guide

Interfacing

The pin-out tables are displayed with the pins in the same relative order as the actual connectors. The pin definitions are defined with noise immunity in mind. The pairs are chosen to match standard SCSI II/III cable pairing to allow a low cost commercial cable to be used for the interface.

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power-consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. Connecting external voltage to the PMC Parallel 485 when it is not powered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time. Alternatively, the use of OPTO-22 isolation panels is recommended.

Keep cables short. Flat cables, even with alternate ground lines, are not suitable for long distances. The PMC BiSerial-II does not contain special input protection. The connector is pinned out for a standard SCSI II/III cable to be used. The twisted pairs are defined to match up with the PMC Parallel 485 pin definitions. It is suggested that this standard cable be used for most of the cable run.

Terminal Block. We offer a high quality 68-screw terminal block that directly connects to the SCSI II/III cable. The terminal block can mount on standard DIN rails. HDEterm68 **[http://www.dyneng.com/HDEterm68.html]**

We provide the components. You provide the system. Safety and reliability can be achieved only by careful planning and practice. Inputs can be damaged by static discharge, or by applying voltage outside of the RS-485 devices rated voltages**.**

Construction and Reliability

PMC Modules were conceived and engineered for rugged industrial environments. The Parallel-485 is constructed out of 0.062 inch thick FR4 material.

Through hole and surface mounting of components are used. IC sockets use gold plated screw machine pins. High insertion and removal forces are required, which assists in the retention of components. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the corner pins of each socketed IC into the socket, using a grounded soldering iron.

The PMC Module connectors are keyed and shrouded with Gold plated pins on both plugs and receptacles. They are rated at 1 Amp per pin, 100 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The PMC is secured against the carrier with the connectors and front panel. If more security against vibration is required the stand-offs can be secured against the carrier.

The PMC Module provides a low temperature coefficient of 0.89 $W/^{o}C$ for uniform heat. This is based upon the temperature coefficient of the base FR4 material of 0.31 $W/m\text{-}^{o}C$, taking into account the thickness and area of the PMC. The coefficient means that if 0.89 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The PMC-PARALLEL-485 design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create a higher power dissipation with the externally connected logic. If more than one Watt is required to be dissipated due to external loading then forced air cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.

Warranty and Repair

Dynamic Engineering warrants this product to be free from defects in workmanship and materials under normal use and service and in its original, unmodified condition, for a period of one year from the time of purchase. If the product is found to be defective within the terms of this warranty, Dynamic Engineering's sole responsibility shall be to repair, or at Dynamic Engineering's sole option to replace, the defective product. The product must be returned by the original customer, insured, and shipped prepaid to Dynamic Engineering. All replaced products become the sole property of Dynamic Engineering.

Dynamic Engineering's warranty of and liability for defective products is limited to that set forth herein. Dynamic Engineering disclaims and excludes all other product warranties and product liability, expressed or implied, including but not limited to any implied warranties of merchandisability or fitness for a particular purpose or use, liability for negligence in manufacture or shipment of product, liability for injury to persons or property, or for any incidental or consequential damages.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
435 Park Dr.
Ben Lomond, CA 95005
831-336-8891
831-336-3840 fax
E-Mail Address support@dyneng.com

Specifications

Logic Interface:	PMC Logic Interface [PCI 33/32]
Digital Parallel IO:	32 differential IO channels. Each with direction control. Additional External Clock input and External Clock Enable.
CLK rates supported:	Multiple rate divisors supplied based on PCI, External, or board mounted oscillator.
Software Interface:	Control Registers, IO registers, IO Read-Back registers
Initialization:	Hardware Reset forces all registers to 0.
Access Modes:	LW aligned
Access Time:	1 PCI wait state
Interrupt:	Edge or Level Detect on any of the 32 IO lines
DMA:	No DMA Support implemented at this time
Onboard Options:	All Options are Software Programmable
Interface Options:	68 Pin SCSI III connector via front panel User IO routed to Pn4
Dimensions:	Standard Single PMC Module.
Construction:	FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components. Programmable parts are socketed.
Temperature Coefficient:	0.89 W/^{O}C for uniform heat across PMC
Power:	Typical 300 mA @ 5V

Order Information

standard temperature range 0-70ºC	
PMC-PARALLEL-485	PMC Module with 32 differential IO channels plus External clock and External Clock En.
PMC-PARALLEL-485-ET	extended temperature version PMC Module with 32 differential IO channels plus External clock an External Clock En. –20 – 85 with switch, -40 – 85 no dipswitch http://www.dyneng.com/pmc_parallel_485.html
PMC-PARALLEL-485-ENG	Engineering kit with reference software, schematic, cable and terminal block. http://www.dyneng.com/HDEterm68.html http://www.dyneng.com/HDEcabl68.html